LISTING OF THE CLAIMS:

Claims 1-22 (cancelled)

23. (Currently Amended) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide which includes an additive or Ge, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, wherein said Si-Ge interlayer has a thickness less than about 3.0 nm. ~~where said Si-Ge interlayer has a Ge concentration ranging from about .01 atomic percent to about 9.0 atomic percent.~~

24. (Withdrawn) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of Ni monosilicide, wherein said substrate and said first layer are separated by a Si-Ge interlayer.

25. (Previously Presented) The electrical contact of Claim 23 wherein said silicon-containing semiconductor material comprises single crystal Si, polycrystalline Si, SiGe, amorphous Si or a silicon-on-insulator (SOI).

26. (Previously Presented) The electrical contact of Claim 23 wherein said metal of said disilicide is Co and said metal silicide is Co disilicide.

27. (Previously Presented) The electrical contact of Claim 23 wherein said metal of said disilicide is Ti and said metal silicide is $TiSi_2$.

28. (Previously Presented) The electrical contact of Claim 27 wherein said $TiSi_2$ is in the C54 phase.

Claims 29-30 (Cancelled)

31. (Previously Presented) The electrical contact of Claim 23 wherein said substrate is doped.

32. (Withdrawn) The electrical contact of Claim 24 wherein said silicon-containing semiconductor material comprises single crystal Si, polycrystalline Si, SiGe, amorphous Si or a silicon-on-insulator (SOI).

33. (Withdrawn) The electrical contact of Claim 24 further comprising an oxide layer present near a surface of said substrate.

34. (Withdrawn) The electrical contact of Claim 33 wherein said oxide layer has a thickness of from about 0.1 to about 3.0 nm.

35. (Withdrawn) The electrical contact of Claim 24 wherein said substrate is doped.

36. (Previously Presented) The electrical contact of Claim 23 wherein said additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh,

Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

37. (Previously Presented) The electrical contact of Claim 36 wherein said additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt or mixtures thereof.

38. (Previously Presented) The electrical contact of Claim 37 wherein said additive is Si, Ti, V, Cr, Ni, Nb, Rh, Ta, Re, Ir or mixtures thereof.

39. (Previously Presented) The electrical contact of Claim 23 wherein said additive is present in said metal disilicide in an amount of from about 0.01 to about 50 atomic percent.

40. (Currently Amended) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material; and

a first layer of metal disilicide ~~having lateral edges~~, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer positioned on an interface between said first layer and said substrate, wherein said Si-Ge interlayer does not substantially extend beyond said interface ~~said Si-Ge interlayer having lateral edges which do not substantially extend beyond the lateral edges of the metal disilicide~~..

41. (Cancelled)